5473/7473 Dual J-K Master-Slave Flip-Flop with Clear

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package			
		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF
T.I.						SN54H73	J①			W①	SN54LS73	J①			W①	SN5473	J①			W①	SN54L73	J①	N①	T①	
						SN74H73	J①	N①			SN74LS73	J①	N①			SN7473	J①	N①			SN74L73	J①	N①	T①	
FAIRCHILD						FM54H73/FM9H73	D①			F①	FM54LS73/FM9LS73					FM5473/FM9N73	D①			F①					
						FC74H73/FC9H73	D①	P①			FC74LS73/FC9LS73					FC7473/FC9N73	D①	P①							
MOTOROLA						MC3163	L①			F①						MC5473	L①			F①					
						MC3063	L①	P①		F①	SN74LS73		P①			MC7473	L①	P①		F①					
N.S.C.						DM54H73	J①	N①			DM54LS73		P①			DM5473	J①	N①		W①	DM54L73	J①	N①		F①
						DM74H73	J①	N①			DM74LS73		P①			DM7473	J①	N①			DM74L73	J①	N①		F①
PHILIPS						N74H73		①			N74LS73		①			FJJ121/7473		①							
SIGNETICS						S54H73	F①	A①		W①						S5473	F①	A①		W①					
						N74H73	F①	A①			N74LS73		A①			N7473	F①	A①							
SIEMENS																FLJ121		①							
FUJITSU																									
HITACHI											HD74LS73		P①			HD7473/HD2515	①	P①							
MITSUBISHI											M74LS73		P①			M53273		P①							
NEC																μPB225	D①	C①							
TOSHIBA																TD3473A		P①							

Electrical Characteristics SN54LS73/SN74LS73A

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7V	Operating free-air temperature range	SN54LS	−55°C to 125°C
Input voltage	5.5V		SN74LS	0°C to 70°C
		Storage temperature range		−65°C to 150°C

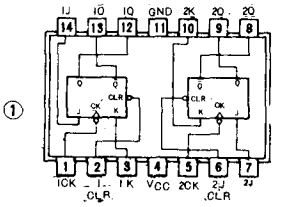
recommended operating conditions

		SN54LS73A			SN74LS73A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Pulse width, t_w	Clock high	20			20			ns
	Preset or clear low	25			25			
Input setup time, t_{setup}	High-level data	20↓			25↑			ns
	Low-level data	20↓			20↑			
Input hold time, t_{hold}		0↓			5↑			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER*			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage		V_{CC}=MIN, I_I=−18mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=MAX	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, I_{OL}=4mA		0.25	0.4	V
I_I	Input current at maximum input voltage	D, J, K	V_{CC}=MAX, V_I=7V			0.1	mA
		Clear				0.3	
		Preset				0.3	
		Clock				0.4	
I_{IH}	High-level input current	D, J, K	V_{CC}=MAX, V_I=2.7V			20	μA
		Clear				60	
		Preset				60	
		Clock				80	
I_{IL}	Low-level input current	D, J, K	V_{CC}=MAX, V_I=0.4V			−0.4	mA
		Clear				−0.8	
		Preset				−0.8	
		Clock				−0.8	
I_{OS}	Short-circuit output current◆	Series 54LS	V_{CC}=MAX	−20		−100	mA
		Series 74LS		−20		−100	
I_{CC}	Supply current (Average per flip-flop)		V_{CC}=MAX, See Note 1		4	6	mA
f_{max}	maximum clock frequency		V_{CC}=5V, T_A=25°C, C_L=15pF, R_L=2kΩ	30	45		MHz
t_{PLH}	from clear, preset or clock (as appropriate) to Q or $\bar{Q}$				15	20	ns
t_{PHL}	from clear, preset or clock (as appropriate) to Q or $\bar{Q}$				15	20	

Pin Assignment (Top View)



Function Tables

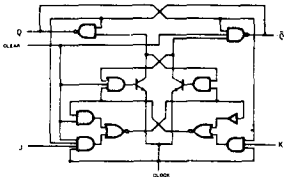
'73 H73, 'L73 (See Note 2)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⊓	L	L	Q_0	$\bar{Q}_0$
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	TOGGLE	

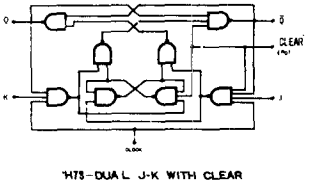
LS73 (See Note 2)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

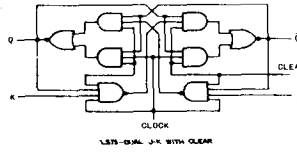
Functional Block Diagrams



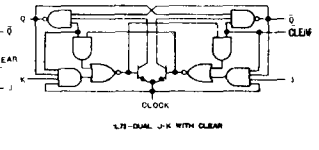
'73-DUAL J-K WITH CLEAR



'H73-DUAL J-K WITH CLEAR



'L73-DUAL J-K WITH CLEAR



'L73-DUAL J-K WITH CLEAR

NOTES: 1. with all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time time of mesaurement, the clock input is grounded.

2. H = high level (steady state), L = low level (steady state), X = irrelevant
↓ = transition from high to low level
⊓ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the of the pulse.
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previons level on each active transition (pulse) of the clock.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC}=5V, T_A=25°C.
◆ Not more than one output should be shorted at time.
*t_{PLH} ≡ propagation delay time, low-to-high-level output;
t_{PHL} ≡ propagation delay time, high-to-low-level output.
§ ↓↑ The arrow indicates the edge of the clock pulse used for refence: ↑ for the rising edge, ↓ for the falling edge.